ABSTRACT

A system and method are provided for testing electronic devices. Generally, the system includes: (i) a pattern memory with outputs for storing and outputting bits to the device; and (ii) a pattern scrambler for coupling bits from the outputs to pins on the device to provide a test pattern to the device having a width of from 1 bit to a width equal to the number of outputs. Preferably, the system includes a clock with a clock cycle, and the scrambler can change the width and/or depth of the test pattern on a cycle-by-cycle basis More preferably, the scrambler can change the bits coupled to one or more of the pins on a cycle-by-cycle basis. In one embodiment, the memory simultaneously provides logic vector memory and scan memory for storing logic and scan vectors respectively, and the width/depth of the vectors can be changed on a cycle-by-cycle basis.